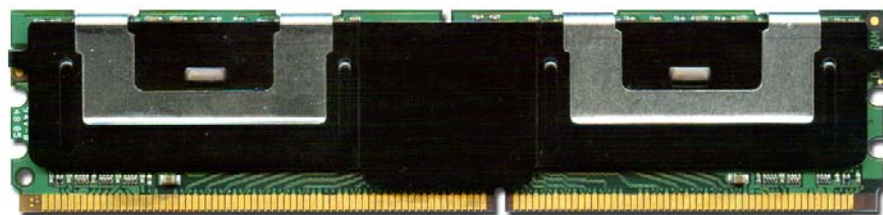


# DTM65536B

**2 GB - 240-Pin DDR2 Low Power FB-DIMM**



## Identification

DTM65536B 256Mx72  
2GB 2Rx8 PC2-5300F-555-11-B0

## Performance range

Clock / Module Speed / CL-t<sub>RCD</sub> -t<sub>RP</sub>  
333MHz / DDR2-667 / 5-5-5  
267MHz / DDR2-533 / 4-4-4  
200MHz / DDR2-400 / 3-3-3

## Features

240-pin JEDEC-compliant DIMM, 133.35 mm wide by 30.35 mm high  
Data Transfer Rate: 5.3 Gigabytes/sec  
Operating Voltage: VDD = 1.8 V ±0.1; VCC = 1.5V ±0.1  
SMBus interface to AMB for configuration register access  
MBIST and IBIST test functions  
Transparent mode for DDR2 SDRAM test support  
Full DIMM Heat Spreader  
High-speed differential point-to-point link  
Fully RoHS Compliant

## Description

The DTM65536B is a Dual Rank PC2-5300 Fully Buffered 256MX72 ECC DIMM that conforms to the JEDEC FB-DIMM standard. Each rank is comprised of nine Samsung 128Mx8 DDR2 DRAMs. One IDT (Rev L4) Advanced Memory Buffer (AMB) is used as the interface between the system memory bus and DIMM DRAMs. One 2K-bit EEPROM is used for Serial Presence Detect. For improved thermal performance, a Full DIMM Heat Spreader with thermal interface material (TIM) is attached to the front and back of the DIMM.

This is a reduced power module. Components have been tested and selected for this design with the lowest power consumption.

## Pin Configurations

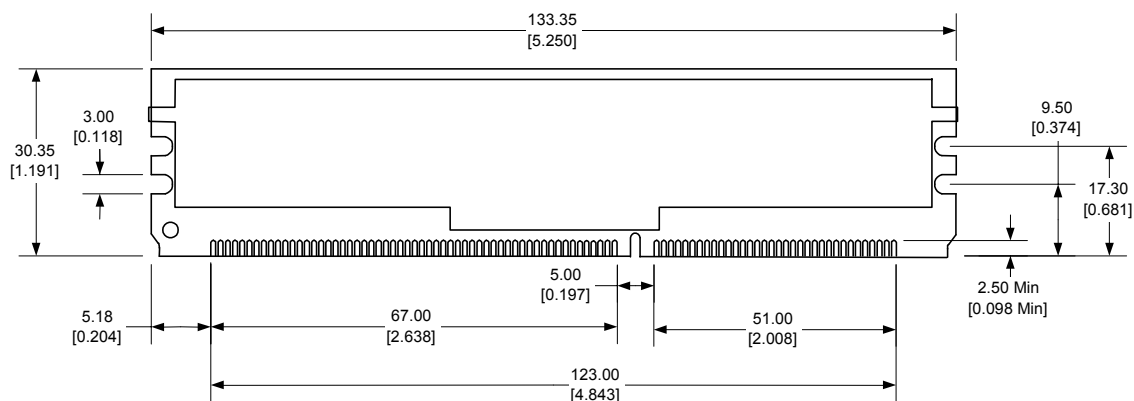
Front side					Back side				
1 VDD	31 PN3	61 /PN9	91 /PS9	121 VDD	151 SN3	181 /SN9	211 /SS9		
2 VDD	32 /PN3	62 VSS	92 VSS	122 VDD	152 /SN3	182 VSS	212 VSS		
3 VDD	33 VSS	63 PN10	93 PS5	123 VDD	153 VSS	183 SN10	213 SS5		
4 VSS	34 PN4	64 /PN10	94 /PS5	124 VSS	154 SN4	184 /SN10	214 /SS5		
5 VDD	35 /PN4	65 VSS	95 VSS	125 VDD	155 /SN4	185 VSS	215 VSS		
6 VDD	36 VSS	66 PN11	96 PS6	126 VDD	156 VSS	186 /SN11	216 SS6		
7 VDD	37 PN5	67 /PN11	97 /PS6	127 VDD	157 SN5	187 /SN11	217 /SS6		
8 VSS	38 /PN5	68 VSS	98 VSS	128 VSS	158 /SN5	188 VSS	218 VSS		
9 VCC	39 VSS	69 VSS	99 PS7	129 VCC	159 VSS	189 VSS	219 SS7		
10 VCC	40 PN13	70 PS0	100 /PS7	130 VCC	160 SN13	190 SS0	220 /SS7		
11 VSS	41 /PN13	71 /PS0	101 VSS	131 VSS	161 /SN13	191 /SS0	221 VSS		
12 VCC	42 VSS	72 VSS	102 PS8	132 VCC	162 VSS	192 VSS	222 SS8		
13 VCC	43 VSS	73 PS1	103 /PS8	133 VCC	163 VSS	193 SS1	223 /SS8		
14 VSS	44 RFU	74 /PS1	104 VSS	134 VSS	164 RFU1	194 /SS1	224 VSS		
15 VTT	45 RFU	75 VSS	105 RFU2	135 VTT	165 RFU1	195 VSS	225 RFU2		
16 VID1	46 VSS	76 PS2	106 RFU2	136 VID0	166 VSS	196 SS2	226 RFU2		
17 /RESET	47 VSS	77 /PS2	107 VSS	137 M_TEST	167 VSS	197 /SS2	227 VSS		
18 VSS	48 PN12	78 VSS	108 VDD	138 VSS	168 SN12	198 VSS	228 SCK		
19 RFU2	49 /PN12	79 PS3	109 VDD	139 RFU2	169 /SN12	199 SS3	229 /SCK		
20 RFU2	50 VSS	80 /PS3	110 VSS	140 RFU2	170 VSS	200 /SS3	230 VSS		
21 VSS	51 PN6	81 VSS	111 VDD	141 VSS	171 SN6	201 VSS	231 VDD		
22 PN0	52 /PN6	82 PS4	112 VDD	142 SN0	172 /SN6	202 SS4	232 VDD		
23 /PN0	53 VSS	83 /PS4	113 VDD	143 /SN0	173 VSS	203 /SS4	233 VDD		
24 VSS	54 PN7	84 VSS	114 VSS	144 VSS	174 SN7	204 VSS	234 VSS		
25 PN1	55 /PN7	85 VSS	115 VDD	145 SN1	175 /SN7	205 VSS	235 VDD		
26 /PN1	56 VSS	86 RFU1	116 VDD	146 /SN1	176 VSS	206 RFU1	236 VDD		
27 VSS	57 PN8	87 RFU1	117 VTT	147 VSS	177 SN8	207 RFU1	237 VTT		
28 PN2	58 /PN8	88 VSS	118 SA2	148 SN2	178 /SN8	208 VSS	238 VDDSPD		
29 /PN2	59 VSS	89 VSS	119 SDA	149 /SN2	179 VSS	209 VSS	239 SA0		
30 VSS	60 PN9	90 PS9	120 SCL	150 VSS	180 SN9	210 SS9	240 SA1		

NOTE: M\_TEST is not used

## Pin Names

Pin Names	Function
SCK, /SCK	System Clock Input
PN, /PN[13:0]	Primary Northbound Data
PS, /PS[9:0]	Primary Southbound Data
SN, /SN[13:0]	Secondary Northbound Data
SS, /SS[9:0]	Secondary Southbound Data
SCL	Serial Clock, EEPROM
SDA	Serial Data, EEPROM
/RESET	AMB Reset Signal
VCC	AMB Core Power and AMB Channel Interface Power (1.5 V)
VDD	DRAM Power and AMB DRAM I/O Power (1.8 V)
VTT	DRAM Address/Command/Clock Termination Power (VDD/2)
VDDSPD	SPD Power
VSS	Ground
RFU	Reserved For Future Use
DNU	Do Not Use
M_TEST	Margin Test
SA[2:0]	Serial Address, EEPROM

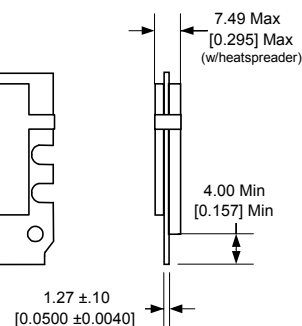
### Front view



### Back view



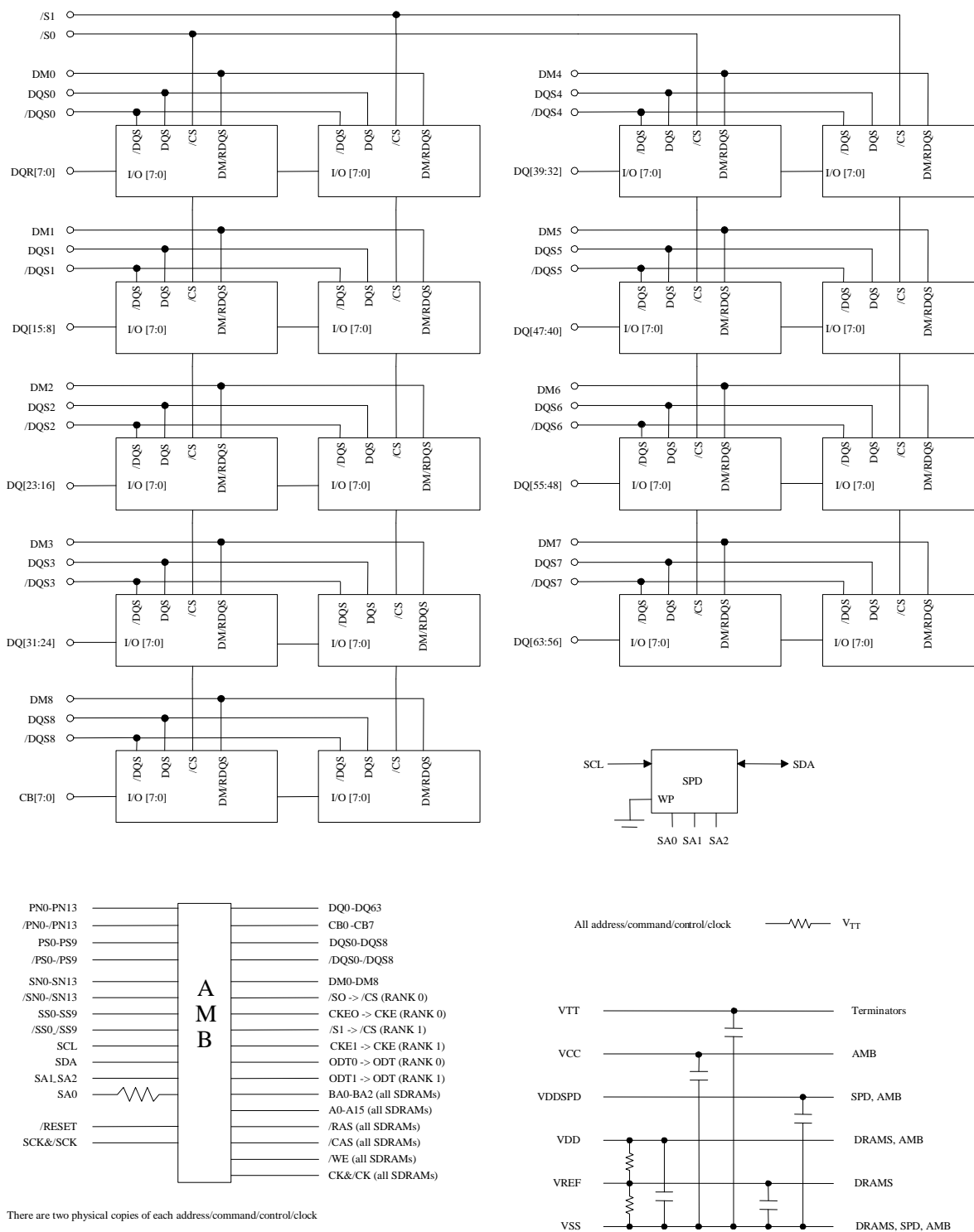
### Side view



### Notes

Tolerances on all dimensions except where otherwise indicated are  $\pm .13$  [.005].

All dimensions are expressed: millimeters [inches]



### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Temperature, DDR2 DRAM Case	$T_{Case}$	0 to +95	C	1, 2
Temperature, Storage	$T_{STG}$	-55 to +100	C	1
Voltage on any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.3 to 1.75	V	1
Voltage on $V_{CC}$ relative to $V_{SS}$	$V_{CC}$	-0.3 to 1.75	V	1
Voltage on $V_{DD}$ relative to $V_{SS}$	$V_{DD}$	-0.5 to 2.3	V	1
Voltage on $V_{TT}$ relative to $V_{SS}$	$V_{TT}$	-0.5 to 2.3	V	1
Power Dissipation	$P_D$	21	W	1

#### NOTES:

1. Operation at or above absolute maximum rating can adversely affect device reliability.
2. For  $85\text{ C} < T_{Case} \leq 95\text{ C}$ ,  $t_{REF1} = 3.9\text{ }\mu\text{s}$  max.

### DC Operating Conditions ( $T_A = 0$ to $70\text{ C}$ , Voltage referenced to $V_{SS} = 0\text{V}$ )

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Note
AMB Supply Voltage	$V_{CC}$	1.425	1.5	1.59	V	
DDR2 Supply Voltage	$V_{DD}$	1.7	1.8	1.9	V	
Termination Voltage	$V_{TT}$	$0.48 \times V_{DD}$	$0.50 \times V_{DD}$	$0.52 \times V_{DD}$	V	
EEPROM Supply Voltage (SPD)	$V_{DDSPD}$	3.0	3.3	3.6	V	
Input High Voltage (SPD)	$V_{IH(DC)}$	2.1		$V_{DDSPD}$	V	1
Input Low Voltage (SPD)	$V_{IL(DC)}$	1.0			V	1
Input High Voltage (RESET/BFUNC)	$V_{IH(DC)}$	1.0			V	2
Input Low Voltage( RESET/BFUNC)	$V_{IL(DC)}$			0.5	V	1
Leakage Curent (RESET/BFUNC)	$I_L$	-90		90	$\mu\text{A}$	2
Leakage Curent (Link)	$I_L$	-5		5	$\mu\text{A}$	

#### Notes:

1. Applies to SMB and SPD bus signals.
2. Applies to AMB CMOS signal /RESET.

### Differential Transmitter Output Specification

Parameter	Symbol	MIN	MAX	Units
Differential peak-to-peak output voltage for large voltage swing $V_{TX-DIFFp-p} = 2 *  V_{TX-D+} - V_{TX-D-} $	$V_{TX-DIFFp-p\_L(1)}$	900	1300	mV
Differential peak-to-peak output voltage for regular voltage swing $V_{TX-DIFFp-p} = 2 *  V_{TX-D+} - V_{TX-D-} $	$V_{TX-DIFFp-p\_R(1)}$	800	---	mV
Differential peak-to-peak output voltage for small voltage swing $V_{TX-DIFFp-p} = 2 *  V_{TX-D+} - V_{TX-D-} $	$V_{TX-DIFFp-p\_S(1)}$	520	---	mV
DC common mode output voltage for large voltage swing Defined as: $V_{TX-CM} = DC(ave)$ of $ V_{TX-D+} + V_{TX-D-} /2$	$V_{TX-CM\_L(1)}$	---	375	mV
DC common mode output voltage for small voltage swing Defined as: $V_{TX-CM} = DC(ave)$ of $ V_{TX-D+} + V_{TX-D-} /2$	$V_{TX-CM\_S(1)}$	135	280	mV
De-emphasized differential output voltage ratio for -3.5 dB de-emphasis -	$V_{TX-DE-3.5-Ratio(1,2,3)}$	-3	-4	dB
De-emphasized differential output voltage ratio for -6 dB de-emphasis	$V_{TX-DE-6-Ratio(1,2,3)}$	-5	-7	dB
AC peak-to-peak common mode output voltage for large swing $V_{TX-CM-AC} = Max  V_{TX-D+} + V_{TX-D-} /2 - Min  V_{TX-D+} + V_{TX-D-} /2$	$V_{TX-CM-ACp-p\_L(1,4)}$	---	90	mV
AC peak-to-peak common mode output voltage for regular swing $V_{TX-CM-AC} = Max  V_{TX-D+} + V_{TX-D-} /2 - Min  V_{TX-D+} + V_{TX-D-} /2$	$V_{TX-CM-ACp-p\_R(1,4)}$	---	80	mV
AC peak-to-peak common mode output voltage for small swing $V_{TX-CM-AC} = Max  V_{TX-D+} + V_{TX-D-} /2 - Min  V_{TX-D+} + V_{TX-D-} /2$	$V_{TX-CM-ACp-p\_S(1,4)}$	---	70	mV
Maximum single-ended voltage in EI condition, DC + AC	$V_{TX-IDLE-SE(5,6)}$	---	50	mV
Maximum single-ended voltage in EI condition, DC only	$V_{TX-IDLE-SE-DC(5,6,7)}$	---	20	mV
Maximum peak-to-peak differential voltage in EI condition	$V_{TX-IDLE-DIFFp-p(6)}$	---	40	mV
Single-ended voltage(w.r.t. VSS) on D+/D-	$V_{TX-SE(1,7)}$	-75	750	mV
Minimum TX eye width, 3.2 and 4 Gb/s	$TTX-Eye-MIN(1,9,10)$	0.7	---	UI
Maximum TX deterministic jitter, 3.2 and 4 Gb/s	$TTX-DJ-DD(1,9,10,11)$	---	0.2	UI
Instantaneous pulse width	$TTX-PULSE(12)$	0.85	---	UI
Differential TX output rise/fall time Given by 20%-80% voltage levels	$TTX-RISE, TTX-FALL(1)$	30	90	ps
Mismatch between rise and fall times	$TTX-RF-MISMATCH$	---	20	ps
Differential return loss Measured over 0.1 GHz to 2.4GHz	$RLTX-DIFF$	8	---	dB
Common mode return loss Measured over 0.1 GHz to 2.4GHz	$RLTX-CM$	6	---	dB
Transmitter termination resistance	$RTX(13)$	41	55	$\Omega$
D+/D- TX resistance difference $RTX-Match-DC = 2 *  RTX-D+ - RTX-D-  / (RTX-D+ + RTX-D-)$ Bounds are applied separately to high and low output voltage states	$RTX-Match-DC$		4	%
Lane-to-lane skew at TX	$LTX-SKEW\_1(14,16)$	---	100+3UI	ps
Lane-to-lane skew at TX	$LTX-SKEW\_2(15,16)$	---	100+2UI	ps
Maximum TX Drift (resync mode)	$TTX-DRIFT-RESYNC(17)$	---	240	ps
Maximum TX Drift (resample mode only)	$TTX-DRIFT-RESAMPLE(17)$	---	120	ps
Bit Error Ratio	$BER(18)$	---	$10^{-12}$	

### NOTES FOR TRANSMITTER OUTPUT SPECIFICATIONS:

1. Specified at the package pins into a timing and voltage compliance test load. Common-mode measurements to be performed using a 101010 pattern.
2. This is the ratio of the  $V_{TX-DIFFp-p}$  of the second and following bits after a transition divided by the  $V_{TX-DIFFp-p}$  of the first bit after a transition.
3. De-emphasis is disabled in the calibration state.
4. Includes all sources of AC common mode noise
5. Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition.
6. Specified at the package pins into a voltage compliance test load. Transmitters must meet both single-ended and differential output E1 specifications.
7. This specification, considered with  $V_{RX-IDLE-SE-DC}$ , implies a maximum 15mV single-ended DC offset between Tx and Rx pins during the electrical idle condition. This in turn allows a ground offset between adjacent FB-DIMM agents of 26mV when worst-case termination resistance matching is considered.
8. The maximum value is specified to be at least  $(V_{TX-DIFFp-p} L / 4) + V_{TX-CM L} + (V_{TX-CM-ACp-p} / 2)$
9. This number does not include the effects of SSC or reference clock jitter.
10. These timing specifications apply to resync mode only.
11. Defined as the dual-dirac deterministic jitter as described in Section 4 of the JEDEC FB-DIMM High Speed Differential PTP Link Draft Spec rev 0.8.
12. Pulse width measured at 0V differential.
13. The termination small signal resistance; tolerance across voltages from 100mV to 400mV shall not exceed  $\pm 5\%$  with regard to the average of the values measured at 100mV and at 400mV for that pin.
14. Lane to Lane skew at the Transmitter pins for an end component.
15. Lane to Lane skew at the Transmitter pins for an intermediate component (assuming zero Lane to Lane skew at the Receiver pins of the incoming PORT).
16. This is a static skew. A FB-DIMM component is not allowed to change its lane to lane phase relationship after initialization.
17. Measured from the reference clock edge to the center of the output eye. This specification is met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.
18. BER per differential lane. For a complete definition of Bit Error Ratio, refer to JEDEC's Compliance Methodology section.

### Differential Receiver Input Specification

Parameter	Symbol	MIN	MAX	Units
Differential peak-to-peak input voltage $VRX-DIFF_{p-p} = 2 *  VRX-D+ - VRX-D- $	$VRX-DIFF_{p-p\_L}(1)$	170	1300	mV
Maximum single-ended voltage for EI condition, DC + AC	$VRX-IDLE-SE(2,3,4)$	---	65	mV
Maximum single-ended voltage for EI condition, DC only	$VRX-IDLE-SE-DC(2,3,4,5)$	---	35	mV
Single-ended voltage (w.r.t. VSS) on D+/D-	$VRX-SE(4)$	-300	900	mV
Single-pulse peak differential input voltage	$VRX-DIFF-PULSE(4,6)$	85	---	mV
Amplitude ratio between adjacent symbols $1100mV < VRX-DIFF_{p-p} \leq 1300mV$	$VRX-DIFF-ADJ-RATIO-HI(4,7)$	---	3	
Amplitude ratio between adjacent symbols $VRX-DIFF_{p-p} \leq 1100mV$	$VRX-DIFF-ADJ-RATIO(4,7)$	---	4	
Maximum RX inherent timing error, 3.2 and 4 Gb/s	$TRX-TJ-MAX(4,8,9)$	---	0.4	UI
Maximum RX inherent deterministic timing error, 3.2 and 4 Gb/s	$TRX-DJ-DD(4,8,9,10)$	---	0.3	UI
Single-pulse width at zero-voltage crossing	$TRX-PW-ZC(4,6)$	0.55	---	UI
Single-pulse width at minimum-level crossing	$TRX-PW-ML(4,6)$	0.2	---	UI
Differential RX input rise/fall time, given by 20%-80% voltage levels	$TRX-RISE, TRX-FALL$	50	---	ps
Common mode of the input voltage Defined as: $VRX-CM = DC(avg) \text{ of }  VRX-D+ + VRX-D- /2$	$VRX-CM(1,11)$	120	400	mV
AC peak-to-peak common mode of input voltage $VRX-CM-AC = Max  VRX-D+ + VRX-D- /2 - Min  VRX-D+ + VRX-D- /2$	$VRX-CM-AC_{p-p}(1)$	---	270	mV
Ratio of $VRX-CM-AC_{p-p}$ to minimum $VRX-DIFF_{p-p}$	$VRX-CM-EH-Ratio(12)$	---	45	%
Differential return loss Measured over 0.1 GHz to 2.4GHz	$RLRX-DIFF$	9	---	dB
Common mode return loss Measured over 0.1 GHz to 2.4GHz	$RLRX-CM$	6	---	dB
RX termination resistance	$RRX(13)$	41	55	$\Omega$
D+/D- RX resistance difference $RRX-Match-DC = 2 *  RRX-D+ - RRX-D-  / (RRX-D+ + RRX-D-)$	$RRX-Match-DC$	---	4	%
Lane-to-lane PCB skew at RX Lane to Lane PCB skew at the Receiver that must be tolerated.	$LRX-PCB-SKEW(14)$	---	6	UI
Minimum RX Drift Tolerance	$TRX-DRIFT(15)$	400	---	ps
Minimum data tracking 3dB bandwidth	$FTRK(16)$	0.2	---	MHz
Electrical idle entry detect time	$TEI-ENTRY - DETECT(17)$	---	60	ns
Electrical idle exit detect time	$TEI-EXIT-DETECT$	---	30	ns
Bit Error Ratio	$BER(18)$	---	$10^{-12}$	

### NOTES FOR RECEIVER INPUT SPECIFICATIONS:

1. Specified at the package pins into a timing and voltage compliant test setup. Note that signal levels at the pad are lower than at the pin.
2. Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition. Worst-case margins are determined by comparing EI levels with common mode levels during normal operation for the case with transmitter using small voltage swing (see RX Single-ended Electrical Idle Levels and RX Common Mode Levels).
3. Multiple lanes need to detect the EI condition before the device can act upon the EI detection.
4. Specified at the package pins into a timing and voltage compliance test setup.
5. This specification, considered with VTX-IDLE-SE-DC, implies a maximum 15mV single-ended DC offset between TX and RX pins during the electrical idle condition. This in turn allows a ground offset between adjacent FB-DIMM of 26mV when worstcase termination resistance matching is considered.
6. The single-pulse mask provides sufficient symbol energy for reliable RX reception. Each symbol complies with both the single-pulse mask and the cumulative eye mask (see RX Single-Pulse Min Width and Amplitude Mask, Pulse Shifted Early, and RX Single-Pulse Min Width and Amplitude Mask, Pulse Shifted Late).
7. The relative amplitude ratio limit between adjacent symbols prevents excessive inter-symbol interference in the Rx. Each symbol must comply with the peak amplitude ratio with regard to both the preceding and subsequent symbols (see RX Maximum Adjacent Symbol Amplitude).
8. This number does not include the effects of SSC or reference clock jitter.
9. This number includes setup and hold of the RX sampling flop.
10. Defined as the dual-dirac deterministic timing error as described in Section 4.2.2 of the JEDEC FB-DIMM High-Speed Differential PTP Link Draft Spec, rev 0.8.
11. Allows for 15mV DC offset between transmit and receive devices.
12. The received differential signal satisfies both this ratio as well as the absolute maximum AC peak-to-peak common mode specification. For example, if  $V_{RX-DIFFp-p}$  is 200mV, the maximum AC peak-to-peak common mode is the lesser of  $(200\text{ mV} * 0.45 = 90\text{mV})$  and  $V_{RX-CM-ACp-p}$ .
13. The termination small signal resistance; tolerance across voltages from 100mV to 400mV shall not exceed  $\pm 5\%$  with regard to the average of the values measured at 100mV and at 400mV for that pin.
14. This number represents the lane-to-lane skew between TX and RX pins and does not include the transmitter output skew from the component driving the signal to the receiver. This is one component of the end-to-end channel skew in the AMB specification.
15. Measured from the reference clock edge to the center of the input eye. This specification is met across specified voltage and temperature ranges. Drift rate of change is significantly below the tracking capability of the receiver.
16. This bandwidth number assumes the specified minimum data transition density. Maximum jitter at 0.2MHz is 0.05UI.
17. The specified time includes the time required to forward the EI entry condition.
18. BER per differential lane.



### Advanced Memory Buffer FBD Timing/Electrical

Parameter	Symbol	MIN	MAX	Units
EI Assertion Pass-Through Timing	tEI PROPAGATE		4	CLKs
EI Deassertion Pass-Through Timing	tEID		tBitlock	CLKs
EI Assertion Duration	tEI	100		CLKs
Bit Lock Interval	tBITLOCK		119	Frames
Frame Lock Interval	tFRAMELOCK		154	Frames

### Advanced Memory Buffer Latency Parameters

Parameter	Symbol	MIN	MAX	Units	Notes
CMD2DATA = 0x40 (Data Rate = 667)	tC2D_AMB	16.2	19	ns	
CMD2DATA = 0x46 (Data Rate = 667)	tC2D_AMB	17.7	20.5	ns	
Resample Delay (6)	tRESAMPLE	0.9	1.4	ns	1
Resync Delay (7,8,9)	tRESYNC	2	3.2	ns	2

#### NOTES:

1. tRESAMPLE is the delay from the southbound input to the southbound output, or the northbound input to the northbound output when in resample mode, measured from the center of the data eye.
2. tRESYNC is the delay from the southbound input to the southbound output, or the northbound input to the northbound output when in resync mode, measured from the center of the data eye.

**AMB Power Specification** ( $T_A = 0$  to  $70^\circ\text{C}$ , Voltage referenced to  $V_{SS} = 0\text{V}$ )

Parameter	Symbol	Test Condition	Power Supply	Value	Unit
Idle Current	IDD_IDLE_0	Single or last FBDIMM: L0 state, idle (0 BW); primary channel enabled, secondary channel disabled, CKE high; command and address lines stable, DDR2 SDRAM clock active.	1.5 V	1600	mA
			1.8 V	500	
Idle Current	IDD_IDLE_1	First FBDIMM: L0 state, idle (0 BW); primary and secondary channels enabled, CKE high; command and address lines stable, DDR2 SDRAM clock active.	1.5 V	2300	mA
			1.8 V	500	
Active Power	IDD_ACTIVE_1	Active Power L0 state, 50% DRAM BW, 67% read, 33% write, primary and secondary channels enabled, DRAM clock active, CKE HIGH.	1.5 V	2900	mA
			1.8 V	1200	
Active Power	IDD_ACTIVE_2	Active Power, Data Pass Through L0 state, 50% DRAM BW to downstream DIMM, 67% read, 33% write, primary and secondary channels enabled, CKE HIGH, Command and address lines stable, DRAM clock active.	1.5 V	2400	mA
			1.8 V	500	
Training	IDD_TRAINING	Primary and secondary channels enabled; 100% toggle on all channel lanes; DDR2 SDRAM devices idle (0 BW); CKE HIGH, command and address lines stable; DDR2 SDRAM clock active.	1.5 V	2300	mA
			1.8 V	400	

### DRAM AC Characteristics (AC operating conditions unless otherwise noted)

Parameter	Symbol	Min Value	Max Value	Unit	Note
Row Cycle Time	$t_{RC}$	60	-	ns	
Auto Refresh Row Cycle Time	$t_{RFC}$	127.5	-	ns	
Row Active Time	$t_{RAS}$	45	70K	ns	
Row Address to Column Address Delay	$t_{RCD}$	15	-	ns	
Row Active to row Active Delay	$t_{RRD}$	7.5	-	ns	
Column Address to Column Address Delay	$t_{CCD}$	2	-	CLK	
Row Precharge time	$t_{RP}$	15	-	ns	
Write Recovery Time	$t_{WR}$	15	-	ns	
Auto Precharge Write Recovery + Precharge Time	$t_{DAL}$	$(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$	-	ns	
System Clock Cycle Time	$t_{CK}$	3000	8000	ps	
Clock High Level Width	$t_{CH}$	0.48	0.52	CLK	
Clock Low Level Width	$t_{CL}$	0.48	0.52	CLK	
DQ output access time from CK & /CK	$t_{AC}$	-0.450	+0.450	ns	
DQS-Out edge to Clock Edge skew	$t_{DQSCK}$	-0.400	+0.400	ns	
DQS-Out edge to Data-out edge skew	$t_{DQSQ}$	-	0.240	ns	
Data-Out hold time from DQS	$t_{QH}$	$t_{HP} - t_{QHS}$	-	ns	1
Data hold skew factor	$t_{QHS}$	-	0.340	ns	1
Clock Half Period	$t_{HP}$	$\min(t_{CL}, t_{CH})$	-	ns	1
Input Setup Time (fast slew rate)	$t_{IS}$	0.200	-	ns	2,3,5,6
Input Hold Time (fast slew rate)	$t_{IH}$	0.275	-	ns	2,3,5,6
Input Pulse Width	$t_{IPW}$	0.6	-	CLK	6
Write DQS High Level Width	$t_{DQSH}$	0.35	-	CLK	
Write DQS Low Level Width	$t_{DQSL}$	0.35	-	CLK	
CLK to First Rising edge to DQS-In	$t_{DQSS}$	-0.25	+0.25	CLK	
Data-In Setup Time to DQS-In (DQ & DM)	$t_{DS}$	0.100	-	ns	7
Data-In Hold Time to DQS-In (DQ & DM)	$t_{DH}$	0.175	-	ns	7

#### NOTES:

1. This calculation accounts for  $t_{DQSQ}(\max)$ , the pulse width distortion of on-chip and jitter.
2. Data sampled at the rising edges of the clock: A0~A13, BA0~BA2, CKE, /S[1:0], /RAS, /CAS, /WE
3. For command/address input slew rate  $\geq 1.0V/ns$
4. For command/address input slew rate  $\geq 0.5V/ns$  and  $< 1.0V/ns$
5. CK, /CK slew rates are  $\geq 1.0V/ns$
6. These Parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.
7. Data latched at both rising and falling edges of Data Strobes (DQS)

### AC Operating Conditions (AC operating conditions unless otherwise noted)

Parameter	Symbol	Min Value	Max Value	Unit	Note
DQ Input Pulse Width	$t_{DIPW}$	0.35	-	CLK	
Read DQS Preamble Time	$t_{RPRE}$	0.9	1.1	CLK	
Read DQS Postamble Time	$t_{RPST}$	0.4	0.6	CLK	
Write DQS Preamble Hold Time	$t_{WPRE}$	0.35	-	CLK	
Write DQS Postamble Time	$t_{WPST}$	0.4	0.6	CLK	
Mode Register Set Delay	$t_{MRD}$	2	-	CLK	
Exit Self Refresh to Non-Read Command	$t_{XSNR}$	$t_{RFC} + 10$	-	ns	
Exit Self Refresh to Read Command	$t_{XSRD}$	200	-	CLK	
Average Periodic Refresh Interval	$t_{REFI}$	-	7.8	$\mu s$	1
		-	3.9	$\mu s$	2

#### NOTES:

1. For  $0\text{ }^{\circ}\text{C} < T_{Case} \leq 85\text{ }^{\circ}\text{C}$
2. For  $85\text{ }^{\circ}\text{C} < T_{Case} \leq 95\text{ }^{\circ}\text{C}$

### SERIAL PRESENCE DETECT MATRIX

Byte#	Function.	Value	Hex
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage		0x92
	Bit 3 ~ Bit 0. SPD Bytes Used -	176	
	Bit 6 ~ Bit 4. SPD Bytes Total -	256	
	Bit 7. CRC Coverage -	Bytes 0-116	
1	SPD Revision	Rev. 1.1	0x11
2	Key Byte / DRAM Device Type	DDR2 FBDIMM	0x09
3	Voltage Levels of this Assembly		0x12
	Bit 3 ~ Bit 0. Power Supply 1 -	1.5V	
	Bit 7 ~ Bit 4. Power Supply 2 -	1.8V	
4	SDRAM Addressing		0x45
	Bit 1, 0. Number of Banks -	8	
	Bit 5 ~ Bit 3. Column Address Bits -	10	
	Bit 7 ~ Bit 5. Row Address Bits -	14	
5	Module Physical Attributes		0x23
	Bit 3 ~ Bit 0. Module Thickness (mm) -	7<x<=8.0	
	Bit 4 ~ Bit 2. Module Height (mm) -	30<x<=35	
	Bit 7, 6. Reserved	0	
6	Module Type		0x07
	Bit 3 ~ Bit 0. Module Type -	FB-DIMM	
	Bit 7 ~ Bit 4. Reserved	0	
7	Module Organization		0x11
	Bit 3 ~ Bit 0. SDRAM Device Width -	8-Bits	
	Bit 5 ~ Bit 3. Number of Ranks -	2-Rank	
	Bit 7, 6. Reserved	0	
8	Fine Timebase Dividend / Divisor		0x00
	Bit 3 ~ Bit 0. Fine Timebase (FTB) Dividend -	0	
	Bit 7 ~ Bit 4. Fine Timebase (FTB) Divisor -	0	
9	Medium Timebase Dividend.	1 (MTB = 0.25ns)	0x01
10	Medium Timebase Divisor.	4 (MTB = 0.25ns)	0x04
11	SDRAM Minimum Cycle Time (tCKmin).	3.0ns	0x0C
12	SDRAM Maximum Cycle Time (tCKmax).	8.0ns	0x20
13	SDRAM CAS Latencies Supported.		0x33
	Bit 3 ~ Bit 0. Minimum CL (clocks) -	3	
	Bit 7 ~ Bit 4. CL Range (clocks) -	3	
14	SDRAM Minimum CAS Latency Time (tAamin).	15.0ns	0x3C

15	SDRAM Write Recovery Times Supported		0x42
	Bit 3 ~ Bit 0. Minimum WR (clocks) -	2	
	Bit 7 ~ Bit 4. WR Range (clocks) -	4	
16	SDRAM Write Recovery Time (tWR).	15.0ns	0x3C
17	SDRAM Write Latencies Supported		0x42
	Bit 3 ~ Bit 0. Minimum WL (clocks) -	2	
	Bit 7 ~ Bit 4. WL Range (clocks) -	4	
18	SDRAM Additive Latencies Supported.		0x40
	Bit 3 ~ Bit 0. Minimum AL (clocks)-	0	
	Bit 7 ~ Bit 4. AL Range (clocks) -	4	
19	SDRAM Minimum RAS to CAS Delay (tRCD).	15.0ns	0x3C
20	SDRAM Minimum Row Active to Row Active Delay (tRRD).	7.5ns	0x1E
21	SDRAM Minimum Row Precharge Time (tRP).	15.0ns	0x3C
22	SDRAM Upper Nibbles for tRAS and tRC.		0x00
	Bit 3 ~ Bit 0. tRAS Most Significant Nibble -		
	Bit 7 ~ Bit 4. tRC Most Significant Nibble -		
23	SDRAM Minimum Active to Precharge Time (tRAS).	45.0ns	0xB4
24	SDRAM Minimum Active to Active/Refresh Time (tRC).	60.0ns	0xF0
25	SDRAM Minimum Refresh Recovery Time Delay (tRFC), (LSB).	127.5ns	0xFE
26	SDRAM Minimum Refresh Recovery Time Delay (tRFC), (MSB).	127.5ns	0x01
27	SDRAM Minimum Internal Write to Read Command Delay (tWTR).	7.5ns	0x1E
28	SDRAM Minimum Internal Read to Precharge Command Delay (tRTP).	7.5ns	0x1E
29	SDRAM Burst Lengths Supported		0x03
	Bit 0. BL = 4 -	X	
	Bit 1. BL = 8 -	X	
	Bit 6 ~ Bit 2. TBD		
	Bit 7. Burst Chop -		
30	SDRAM Terminations Supported.		0x07
	Bit 0. 150 ohms ODT -	X	
	Bit 1. 75 ohms ODT -	X	
	Bit 2. 50 ohms ODT -	X	
	Bit 6 ~ Bit 3. TBD		
31	SDRAM Drivers Supported.		0x01
	Bit 0. Weak Driver -	X	
	Bit 7 ~ Bit 1. TBD		
32	SDRAM Average Refresh Interval (tREFI) / Double Refresh mode bit / High Temperature self-refresh rate support indication.		0xC2
	Bit 0 ~ Bit 3. Average Refresh Interval (tREFI) uS -	7.8	

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	Bit 5, Bit 4. TBD		0	
	Bit 6. High Temperature Self-Refresh -		1-Required	
	Bit 7. Double Refresh Requirement -		1-Supported	
33	Tcasemax Delta.			0x52
	Bit 3 ~ Bit 0. DT4R4W Delta, Subfield B: 0.4 °C -		0.8	
	Bit 7 ~ Bit 4. Tcasemax, Subfield A: 2 °C -		10	
34	Thermal Resistance of SDRAM Package. °C/W		61	0x7A
35	SDRAM Case Temperature Rise from Ambient due to Activate-Precharge minus 2.8 °C offset temperature (DT0). °C			0x50
	Bit 1, Bit 0. Reserved		0	
	Bit 7 ~ Bit 2. DT0 -		6	
36	SDRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q). °C		4.7	0x2F
37	SDRAM Case Temperature Rise from Ambient due to Precharge Power-Down (DT2P). °C		0.585	0x27
38	SDRAM Case Temperature Rise from Ambient due to Active Standby (DT3N). °C		5.85	0x27
39	SDRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit).			0x4C
	Bit 0. DT4R4W Mode Bit, Subfield B: 0.4 °C		0	
	Bit 7 ~ Bit 1. DT4R, Subfield A: 0.4 °C -		15.2	
40	SDRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B). °C		18.5	0x25
41	SDRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7). °C		20	0x28
42-74	Reserved		UNUSED	0x00
75	QR Control.			0x00
76	QR ODT control for Rank 0 and rank 1 Reads and writes.			0x00
77	QR ODT1 and ODT2 control for reads.			0x00
78	FBD ODT Definition for Rank 2 and 3			0x00
	Bit 1, Bit 0. Rank 2 Data DRAM ODT -		Disabled	
	Bit 3, Bit 2. Rank 2 Ecc DRAM ODT -		Disabled	
	Bit 5, Bit 4. Rank 3 Data DRAM ODT -		Disabled	
	Bit 7, Bit 6. Rank 3 Ecc DRAM ODT -		Disabled	
79	FBD ODT Definition for Rank 0 and 1			0x22
	Bit 1, Bit 0. Rank 0 Data DRAM ODT -		150 Ohms	
	Bit 3, Bit 2. Rank 0 Ecc DRAM ODT -		Disabled	
	Bit 5, Bit 4. Rank 1 Data DRAM ODT -		150 Ohms	
	Bit 7, Bit 6. Rank 1 Ecc DRAM ODT -		Disabled	
80	Reserved		UNUSED	0x00
81	Channel Protocols Supported, Least Significant Byte			0x02

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	Bit 0, DDR2 Base Non-ECC Protocol - 0-Not Supported		
	Bit 1, DDR2 Base ECC Protocol - 1-Supported		
	Bit 7 ~ Bit 2. TBD 0		
82	Channel Protocols Supported, Most Significant Byte	UNUSED	0x00
83	Back-to-back Turnaround Cycles		0x10
	Bit 1, Bit 0. Rank Read-to-Read - 0 add-l clock		
	Bit 3, Bit 2. Write-to-Read - 0 add-l clock		
	Bit 5, Bit 4. Read-to-Write - 1 add-l clock		
	Bit 7, Bit 6. TBD 0		
84	AMB Read Access Time for DDR2-800 (AMB.LINKPARNXT[1:0] = 11)		0x4A
	Bit 3 ~ Bit 0. Read Access Fine Granularity (UI) 10		
	Bit 7 ~ Bit 4. Read Access Coarse Granularity (tCK) 4		
85	AMB Read Access Time for DDR2-667 (AMB.LINKPARNXT[1:0] = 10)		0x46
	Bit 3 ~ Bit 0. Read Access Fine Granularity (UI) 6		
	Bit 7 ~ Bit 4. Read Access Coarse Granularity (tCK) 4		
86	AMB Read Access Time for DDR2-533 (AMB.LINKPARNXT[1:0] = 01)		0x38
	Bit 3 ~ Bit 0. Read Access Fine Granularity (UI) 8		
	Bit 7 ~ Bit 4. Read Access Coarse Granularity (tCK) 3		
87	Thermal Resistance of AMB Package from Top (Case) to Ambient ( Psi T-A AMB ). °C/W	21	0x2A
88	AMB Case Temperature Rise from Ambient due to AMB in Idle_0 State (DT AMB Idle_0). °C	51	0x33
89	AMB Case Temperature Rise from Ambient due to AMB in Idle_1 State (DT AMB Idle_1). °C	64	0x40
90	AMB Case Temperature Rise from Ambient due to AMB in Idle_2 State (DT AMB Idle_2). °C	55	0x37
91	AMB Case Temperature Rise from Ambient due to AMB in Active_1 State (DT AMB Active_1). °C	87	0x57
92	AMB Case Temperature Rise from Ambient due to AMB in Active_2 State (DT AMB Active_2). °C	70	0x46
93	AMB Case Temperature Rise from Ambient due to AMB in L0s State (DT AMB L0s). °C	UNUSED	0x00
94-97	Reserved	UNUSED	0x00
98	AMB Junction Temperature Maximum (Tjmax). °C	125	0x1F
99	Reserved		0x0A
100	Reserved	UNUSED	0x00
101	AMB Personality Bytes: Pre-initialization.		0xA5



102	AMB Personality Bytes: Pre-initialization.		0x02
103	AMB Personality Bytes: Pre-initialization.		0xDA
104	AMB Personality Bytes: Pre-initialization.		0x66
105	AMB Personality Bytes: Pre-initialization.		0x97
106	AMB Personality Bytes: Pre-initialization.		0x9C
107	AMB Personality Bytes: Post-initialization.		0xDB
108	AMB Personality Bytes: Post-initialization.		0x36
109	AMB Personality Bytes: Post-initialization.		0x04
110	AMB Personality Bytes: Post-initialization.		0xAF
111-114	AMB Personality Bytes: Post-initialization.		0xE8
115	AMB Manufacturer's JEDEC ID Code.		0x7F
116	AMB Manufacturer's JEDEC ID Code.		0xB3
117	Module ID: Module Manufacturer's JEDEC ID Code.		0x01
118	Module ID: Module Manufacturer's JEDEC ID Code.		0x91
119	Module ID: Module Manufacturing Location.		0x01
120,121	Module ID: Module Manufacturing Location.		0x00
122-125	Module ID: Module Serial Number.		0x00
126	Cyclical Redundancy Code (CRC).		0x8B
127	Cyclical Redundancy Code (CRC).		0xAB
128-131	Module Part Number		0x20
132	Module Part Number	D	0x44
133	Module Part Number	A	0x41
134	Module Part Number	T	0x54
135	Module Part Number	A	0x41
136	Module Part Number	R	0x52
137	Module Part Number	A	0x41
138	Module Part Number	M	0x4D
139	Module Part Number		0x20
140	Module Part Number	6	0x36
141	Module Part Number	5	0x35
142	Module Part Number	5	0x35
143	Module Part Number	3	0x33
144	Module Part Number	6	0x36
145	Module Part Number		0x20
146,147	Module Revision Code	UNUSED	0x00
148,149	SDRAM Manufacturer's JEDEC ID Code	UNUSED	0x00
150-175	Manufacturer's Specific Data	UNUSED	0x00
176-255	Open for customer use	UNUSED	0x00



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